Dolphin Technology

DOLPHIN TECHNOLOGY PRODUCT OFFERING
DDR PHY DDR CONTROLLER

DDR PHY & DDR CONTROLLER

Dolphin Technology's hardened DDR4/3/2 SDRAM PHY and LPDDR5/4x/4/3/2 SDRAM PHY IP is a silicon-proven. Combo PHY supporting speeds up to 4266 Mbps. It is fully compliant with the DFI 4.0 specification, and features include slew rate control, per-bit de-skew, gate training, read and write leveling and built-in self-test (BIST).

It also complies to Automotive standard AEC-Q100 with Fault coverage 99.8%.
In addition, our PHY IP is optimized to provide a complete solution when combined with Dolphin's DDRx and LPDDRx SDRAM Memory Controller IP.

DDR PHY (HARD IP)	2/3nm	4/5/6/7 nm	12/16 nm	28nm	40nm	55nm	65nm
DDR4/3/2 PHY (DFI 4.0 compliant)	●	●	●	●	●		
LPDDR5/4x/4/3/2 PHY (DFI 4.0 compliant)	●	●	●	●	●		
DDR3/2 PHY (DFI 4.0 compliant)					●	●	●
Maximum speed, with 1.8V oxide (Mbps)	6400	4266	3200	3200	2133	1600	1600
Maximum speed, with 2.5V oxide (Mbps)	1600	1600	1600	1600	1600	1600	1600
IP is split into two hard macros (one for commands, control and address pins, one for 8-bit data bus)			●	●	●	●	●
Supports custom number of address bits			●	●	●	●	●
Compensation controller and pads for automatic driver and receiver termination impedance calibration			●	●	●	●	●
Slew rate control, per-bit de-skew, gate training, read and write leveling			●	●	●	●	●
JTAG signals for Mentor/Synopsys and LogicVision			●	●	●	●	●
BIST with Pseudo Random Pattern Generator			●	●	●	●	●
Loopback mode			●	●	●	●	●
Scannable flops			●	●	●	●	●
Wirebond, flip-chip and cup configurations			●	●	●	●	●

DDR CONTROLLER (SOFT IP)							
DFI 4.0 Interface with Matching, 1:2 or 1:4 Frequency Ratio	●	●	●	●	●	●	●
Built-in Gate Training and Read/Write Leveling	●	●	●	●	●	●	●
Maximum speed (Mbps)	6400	4266	3200	2133	1600	1600	1600
JEDEC Standard DDR4/3/2 and LPDDR4/3/2 SDRAM	●	●	●	●			
JEDEC Standard DDR3/2 and LPDDR2 SDRAM					●	●	●
Multi-port configurable AXI4 interface w/QoS signaling	●	●	●	●	●	●	●
Multi-port arbitration engine with programmable dynamic priority algorithm	●	●	●	●	●	●	●
Pipeline Arbitration Option for Frequency vs. Latency Tradeoff	●	●	●	●	●	●	●
Fully configurable for various performances and requirements	●	●	●	●	●	●	●
FPGA portable (Xilinx PHY & Altera PHY compatible)	●	●	●	●	●	●	●
BFM verification suite	●	●	●	●	●	●	●
Single AXI4-Lite, APB programming interface	●	●	●	●	●	●	●
AXI4 dynamic QoS signaling for non-blocking communications	●	●	●	●	●	●	●
Support for low-latency bypass ports/channels	●	●	●	●	●	●	●

Front End views are available under NDA.

For more information, contact Dolphin Support or sales@dolphin-ic.com

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Advanced dynamic QoS support based on Queuing Theory and Traffic Hysteresis		●	●	●	●	●	●
Sideband and Inline ECC scheme		●	●	●	●	●	●
Dynamic Address Mapping Scheme		●	●	●	●	●	●
Multiple Burst Priority Arbitration Scheme		●	●	●	●	●	●
Internal Intelligent Bank Management and Auto-precharge Scheduling		●	●	●	●	●	●
Intelligent Traffic Direction Aggregation and Switching		●	●	●	●	●	●
Automatic Periodic Refresh, Automatic Periodic ZQ Calibration		●	●	●	●	●	●

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